CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1. (Original) A configuration circuit for a programmable logic device comprising:

a non-volatile memory cell;

a latch circuit coupled to a logic core of the programmable logic device; and

an initialization circuit coupled to the non-volatile memory cell and the latch circuit, wherein the initialization circuit includes:

a first switch element configured to selectively couple the latch circuit to a first voltage supply terminal; and

a second switch element configured to selectively couple the latch circuit to the non-volatile memory cell.

2. (Original) The configuration circuit of Claim 1, wherein the first switch element comprises a p-channel transistor and the first voltage supply terminal provides a positive supply voltage.

3. (Original) The configuration circuit of Claim 2, wherein the second switch element comprises an n-channel transistor.

4. (Original) The configuration circuit of Claim 1, wherein the non-volatile memory cell comprises a memory transistor having a floating gate structure.

5. (Original) The configuration circuit of Claim 4, further comprising means for programming and erasing the floating gate structure.

6. (Original) The configuration circuit of Claim 4, further comprising:

an access transistor;

a tunnel diode coupled to the access transistor and the floating gate structure; and

a capacitor structure coupled to the floating gate structure.

7. (Original) The configuration circuit of Claim 1, wherein the latch circuit comprises a pair of cross-coupled inverters.

8. (Original) The configuration circuit of Claim 1, further comprising a first latch access transistor coupled to the latch circuit.

9. (Original) The configuration circuit of Claim 8, further comprising a second latch access transistor coupled to the latch circuit.

10. (Original) The configuration circuit of Claim 1, further comprising a delay chain for providing a signal to control at least one of the first and second switch elements.

11. (Original) The configuration circuit of Claim 1, wherein the first and second switch elements are coupled to a set control signal.

12. (Original) The configuration circuit of Claim 1, wherein the non-volatile memory cell is an electrically erasable memory cell.

13. (Withdrawn) A method of configuring a programmable logic device comprising:

selectively programming selected memory cells of a group of non-volatile memory cells on the programmable logic device; then

activating a control signal to couple a plurality of latch circuits to a voltage supply terminal; and then

de-activating the control signal to couple each of the latch circuits to a corresponding one of the memory cells.

14. (Withdrawn) The method of Claim 13, further comprising writing a first set of configuration values to the plurality of latch circuits through corresponding direct access transistors.

15. (Withdrawn) The method of Claim 14, wherein the first set of configuration values configures the programmable logic device for testing.

16. (Withdrawn) The method of Claim 14, further comprising writing a second set of configuration values to the plurality of latch circuits through the corresponding direct access transistors.

17. (Withdrawn) The method of Claim 13, further comprising erasing the group of non-volatile memory cells.

18. (Withdrawn) The method of Claim 17, wherein the step of erasing comprises adjusting threshold voltages of the group of non-volatile memory cells such that the group of non-volatile memory cells is non-conductive when a ground supply voltage is applied to the memory cells.

19. (Withdrawn) The method of Claim 18, wherein the step of selectively programming comprises adjusting threshold voltages of the selected memory cells such that the selected memory cells are conductive when a ground supply voltage is applied to the selected memory cells.

20. (Withdrawn) The method of Claim 13, further comprising configuring the programmable logic device in response to contents of the latch circuits.